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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,168	12/18/2001	Ralf Dorscheid	DE000234	5133
24737	7590	11/24/2004	EXAMINER	
PHILIPS INTELLECTUAL PROPERTY & STANDARDS P.O. BOX 3001 BRIARCLIFF MANOR, NY 10510			REIS, TRAVIS M	
			ART UNIT	PAPER NUMBER
			2859	

DATE MAILED: 11/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>		<b>Applicant(s)</b>	
	10/023,168		DORSCHIED ET AL.	
	<b>Examiner</b>		<b>Art Unit</b>	
	Travis M Reis		2859	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 24 August 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-8 and 12-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 and 12-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |                                                                                                                        |                                                                                         |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                            | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____                                                |

## DETAILED ACTION

### *Response to Amendment*

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-4, 6-8 & 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wieczorek et al. (U.S. Patent 6292528) in view of Nakajyo et al. (U.S. Patent 6420213) & Yamamoto et al. (U.S. Patent 6265782).

Wieczorek et al. disclose a detector for the detection of electromagnetic radiation, i.e. X-rays (col. 3 line 10), which detector includes a scintillator (11), a CMOS chip (9), and a base element (15), wherein a respective intermediate layer (13) that is defined in respect of its gap width is arranged each time between the scintillator and the CMOS chip and a layer (16) between the CMOS chip and the basic element, wherein said intermediate layers contains an adhesive (13, 16), wherein said adhesive has some quantities applied to the surface of the scintillator that faces the CMOS chip as well as to bumps that are present on the CMOS chip while said adhesive also has some quantities (16) applied directly to the rear surfaces of the CMOS chip and the basic element .

Wieczorek et al. do not disclose the basic element is a ceramic element based on aluminum oxide. However, the particular type of material used to make the basic element, absent any criticality, is only considered to be the use of a " preferred " or " optimum "

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material out of a plurality of well known materials that a person having ordinary skill in the art at the time the invention was made would have find obvious to provide using routine experimentation based, among other things, on the intended use of Applicant's apparatus, i.e., suitability for the intended use of Applicant's apparatus, and since the courts have stated that a selection of a material on the basis of suitability for intended use of an apparatus would be entirely obvious. See In re Leshin, 125 USPQ 416 (CCPA 1960 ).

Wieczorek et al. do not disclose spacers.

Nakajyo et al. discloses a method for fixing a semiconductor device (1) having stud bumps/spacers (2) to a ceramic substrate (3) by an electrically non-conductive epoxy resin adhesive (7) (col. 6 lines 66-67 through col. 7 line 1), wherein the gap width is determined by the quantity of adhesive and plurality of spacers (Figures 2 & 4). Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention was made to add the stud bumps/spacers disclosed by Nakajyo et al. to the adhesive layers & electric leads, i.e. the layer between the basic element and the CMOS chip; and the layer between the scintillator and the CMOS chip, disclosed by Wieczorek in order to insure the standard flatness between the CMOS chip and bond pad, thereby minimizing the stretch between electrical leads by preventing one side to be higher than the opposite side.

Wieczorek does not disclose a second acrylate adhesive.

Yamamoto et al. discloses a semiconductor device, semiconductor chip mounting substrate, methods of manufacturing the device and substrate, adhesive, and adhesive double coated film using an adhesive comprised of the epoxy-group-containing acrylic copolymer adhesive and an additional epoxy resin used together in order to reduce the number of cracks and since it has an excellent reactivity with the epoxy resin and improves the adhesive film strength (col. 14 lines 46-64). Therefore, it would have been obvious to one

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with ordinary skill in the art at the time of the invention was made to add the epoxy-group-containing acrylic copolymer adhesive disclosed by Yamamoto et al. to the adhesive disclosed by Wieczorek in order to reduce the number of cracks and since it has an excellent reactivity with the epoxy resin and improves the adhesive film strength.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wieczorek et al., Nakajyo et al., & Yamamoto et al. as applied to claims 1-4, 6-8, & 12 above, and further in view of Doyle et al. (U.S. Patent 6063688).

Wieczorek et al., Nakajyo et al., & Yamamoto et al. disclose all of the instant claimed invention as stated above in the rejection of claims 1-4, 6-8, & 12 including the spacers can be made of Au, Al, and solder (Nakajyo et al. col. 7 lines 62-64).

Wieczorek et al., Nakajyo et al., & Yamamoto et al. do not disclose the spacer is a wire.

Doyle et al. discloses the fabrication of deer submicron structures and quantum wire transistors using hard-mark transistor width definition, wherein quantum wires are used as spacers for the formation of gaps/trenches in the substrate surface (col. 7 lines 50 & 55-57). Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention was made to replace the stud bumps disclosed by Wieczorek et al., Nakajyo et al., & Yamamoto et al. with wire, as taught by Doyle et al. since the spacers claimed by Applicant and the spacers used by Wieczorek et al., Nakajyo et al., & Yamamoto et al. are well known alternate types of spacers which will perform the same function, if one is replaced with the other, of creating gaps between the dielectric elements.

#### ***Response to Arguments***

5. Applicant's arguments with respect to claims 1-8 & 12-16 have been considered but are moot in view of the new ground(s) of rejection.

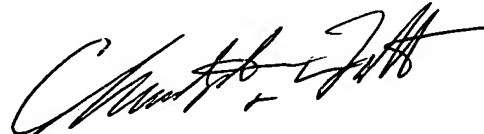
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**Conclusion**

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Travis M Reis whose telephone number is (571) 272-2249. The examiner can normally be reached on 8--5 M--F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on (571) 272-2245. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306 for all communications.

Travis M Reis  
Examiner  
Art Unit 2859



Diego Gutierrez  
Supervisory Patent Examiner  
Technology Center 2800

tmr  
November 19, 2004